PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

13/13 Amdt 8/09/02 A. Waller

In re the Application of

Nobuaki HASHIMOTO

Group Art Unit: 2822

Application No.: 09/856,627

Examiner: I. Soward

Filed: May 24, 2001

Docket No.: 109609

For: INTERCONNECT SUBSTRATE, SEMICONDUCTOR DEVICE, METHOD OF FABRICATING, INSPECTING AND MOUNTING THE SEMICONDUCTOR DEVICE, CIRCUIT BOARD, AND ELECTRONIC INSTRUMENT

AMENDMENT

Director of the U.S. Patent and Trademark Office
Washington, D.C. 20231

Sir:

In reply to the Office Action mailed May 9, 2002, please amend the above-identified application as follows:

IN THE SPECIFICATION:

Page 1, between lines 4 and 5, insert a new paragraph as follows:

-- This application, under 35 U.S.C. §371, is a U.S. National Stage application of PCT/JP00/06624 filed September 29, 2000.--

IN THE CLAIMS:

Please replace claims 1, 13, 15 and 16 as follows:

1. (Amended) An interconnect substrate over which an interconnect pattern is formed, comprising:

a first portion; and

a second portion to be superposed on the first portion,

wherein the first portion has an end part as a positioning reference; and